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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,453	01/16/2002	Bharath Rangarajan	F0595	6507

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EXAMINER	
STAFIRA, MICHAEL PATRICK	
ART UNIT	**PAPER NUMBER**
2877	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,453	RANGARAJAN ET AL.	
	Examiner	Art Unit	
	Michael P. Stafira	2877	

-- The MAILING DATE of this communication appears on the cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,7 are rejected under 35 U.S.C. 102(b) as being anticipated by Silva et al. ('862).

Claim 1

Silva et al. ('862) discloses a light source (Fig. 6, Ref. 32) directed to at least one portion of an ILD layer (Fig. 6, Ref. 10) and a measuring system (Fig. 6, Ref. 34) for measuring parameters of the ILD layer based on light reflected from the at least one portion of the ILD layer (Col. 10, lines 42-48). The reference of Silva et al. ('862) further discloses a processor (Fig. 6, Ref. C) operatively coupled to the measuring system (See Fig. 6), the processor receiving ILD layer parameter data from the measuring system and the processor using the data to determine the presence of a void in the ILD layer (Col. 10, lines 42-48; Col. 1-2, lines 58-6).

Claim 2

The reference of Silva et al. ('862) further discloses a scatterometry system for processing the light reflected from the ILD layer (See Abstract).

Claim 7

The reference of Silva et al. ('862) further discloses that the processor determines the existence of an unacceptable ILD void for at least a portion of the ILD layer based upon the determined ILD void differing from an acceptable value (Col. 10, lines 42-49).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Silva et al. ('862) in view of Subramanian et al. ('753).

Claim 6

Silva et al. ('862) substantially teaches the claimed invention except that it does not show a processor mapping the ILD layer into a plurality of grid blocks, detecting the presence of an ILD void at a grid block, and comparing it to known ILD void values to determined the dimensions of the void. Subramanian et al. ('753) shows that it is known to provide a processor mapping the ILD layer into a plurality of grid blocks, detecting the presence of an ILD void at a grid block, and comparing it to known ILD void values to determined the dimensions of the void (Col. 15-16, lines 40-23) for an apparatus for surface inspection of a wafer. It would have been obvious to combine the device of Silva et al. ('862) with the processor of Subramanian et al. ('753) for the purpose of providing an increased accuracy and location of defects found in the wafer, therefore increasing the quality of the wafers.

3. Claims 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silva et al. ('862) as applied to claim 1 above, and further in view of Kleinknecht et al. ('213).

Claim 3

Silva et al. ('862) substantially teaches the claimed invention except that it does not show the measuring system further measures parameters of the ILD layer based on light passing through the ILD layer. Kleinknecht et al. ('213) shows that it is known to provide a measuring system that measures the parameters of an ILD layer based on light passing through the ILD layer (See Fig. 7) for an optical measuring system. It would have been obvious to combine the device of Silva et al. ('862) with the measuring system of passing light through the ILD layer of Kleinknecht et al. ('213) for the purpose of providing rapid and accurate determination of the widths of fine-line structures.

Claim 4

Silva et al. ('862) further discloses the processor being operatively coupled to the scatterometry system, the processor analyzing data relating to ILD voids received from the scatterometry system, and the processor basing a determination of whether an ILD void exists at least partially on the analyzed data (See Abstract).

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Silva et al. ('862) in view of Kleinknecht et al. ('213) as applied to claim 4 above, and further in view of Subramanian et al. ('753).

Claim 5

Silva et al. ('862) in view of Kleinknecht et al. ('213) substantially teaches the claimed invention except that it does not show the data further relating to thickness of the ILD layer. Subramanian et al. ('753) shows that it is known to provide the data further relating to thickness of the ILD layer (Col. 7, lines 32-37) for an apparatus for the surface inspection of a wafer. It would have been obvious to combine the device of Silva et al. ('862) in view of Kleinknecht et al. ('213) with the data of Subramanian et al. ('753) for the purpose of providing increased information of the size of the defect and how far it has penetrated the layers.

5. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silva et al. ('862) in view of Subramanian et al. ('753).

Claim 8

Silva et al. ('862) discloses the steps of defining an ILD layer as a plurality of portion (typical wafer structure), directing light (Fig. 6, Ref. 32) onto at least one of the portions; collecting light reflected from the at least one portion (See Abstract).

Silva et al. ('862) substantially teaches the claimed invention except that it does not show a reflected light array from the at least one portion to a database, where the database comprises known ILD layers having at least one void present, to determine the presence of the at least one void in the at least one portion associated with the ILD layer, and selectively marking an ILD layer portion as having the at least one void. Subramanian et al. ('753) shows that it is known to provide a reflected light array from the at least one portion to a database, where the database comprises known ILD layers having at least one void present, to determine the presence of the at least one void in the at least one portion associated with the ILD layer, and selectively marking an ILD layer portion as having the at least one void (Col. 15-16, lines 40-23) for an apparatus for measuring the surface of a wafer. It would have been obvious to combine the device of Silva et al. ('862) with the database of Subramanian et al. ('753) for the purpose of providing increased sensitivity in the measurement by using known measurements to compare the measured data.

Claim 9

The reference of Silva et al. ('862) further discloses using a scatterometry system to process the reflected light (See Abstract).

Claim 10

Silva et al. ('862) substantially teaches the claimed invention except that it does not show a processor mapping the ILD layer into a plurality of grid blocks, detecting the presence of an

ILD void at a grid block, and comparing it to known ILD void values to determined the dimensions of the void. Subramanian et al. ('753) shows that it is known to provide a processor mapping the ILD layer into a plurality of grid blocks, detecting the presence of an ILD void at a grid block, and comparing it to known ILD void values to determined the dimensions of the void (Col. 15-16, lines 40-23) for an apparatus for surface inspection of a wafer. It would have been obvious to combine the device of Silva et al. ('862) with the processor of Subramanian et al. ('753) for the purpose of providing an increased accuracy and location of defects found in the wafer, therefore increasing the quality of the wafers.

Claim 11

Silva et al. ('862) discloses a means for detecting ILD void formation in a plurality of portions of the ILD layer and means for selectively marking an ILD layer portion as having a void formed therein (Col. 10, lines 43-48).

Response to Arguments

6. Applicant's arguments, see Response, filed 7/14/2003, with respect to the rejection(s)of claim(s) 1-11 under 102e & 103a have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of claims 1-11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael P. Stafira whose telephone number is 703-308-4837. The examiner can normally be reached on 4/10.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on 703-308-4881. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Michael P. Stafira
Primary Examiner
Art Unit 2877

September 15, 2003